

Silicon Monitoring

On-chip setup slack monitors

Product Brief
Rev 2.1

C0 PUBLIC

Description

The silicon monitoring platform:

- minimizes power consumption
- ensures safe and reliable operation
- cuts production test costs
- enables lifecycle management

The platform accurately monitors the setup slack margin of your digital cores in real-time. This ability to dynamically sense the impact of the process, workload and operating conditions at data level enables (see Fig. 1):

- significant power savings through dynamic optimization of the supply voltage
- prevention of data corruption via ultra-fast triggering of safety mechanisms
- performance maximization by combining the two approaches above
- predictive maintenance thanks to accurate sensing of the aging impacts
- minimization of the design margins and specifications spread

A purely soft IP (synthesizable RTL), the platform integration is:

- fully automated through provided TCL scripts
- compatible with most EDA flows
- totally based on standard cells (see Fig. 3)

The platform comes complete with control, interface and safety subblocks (see Fig. 2).

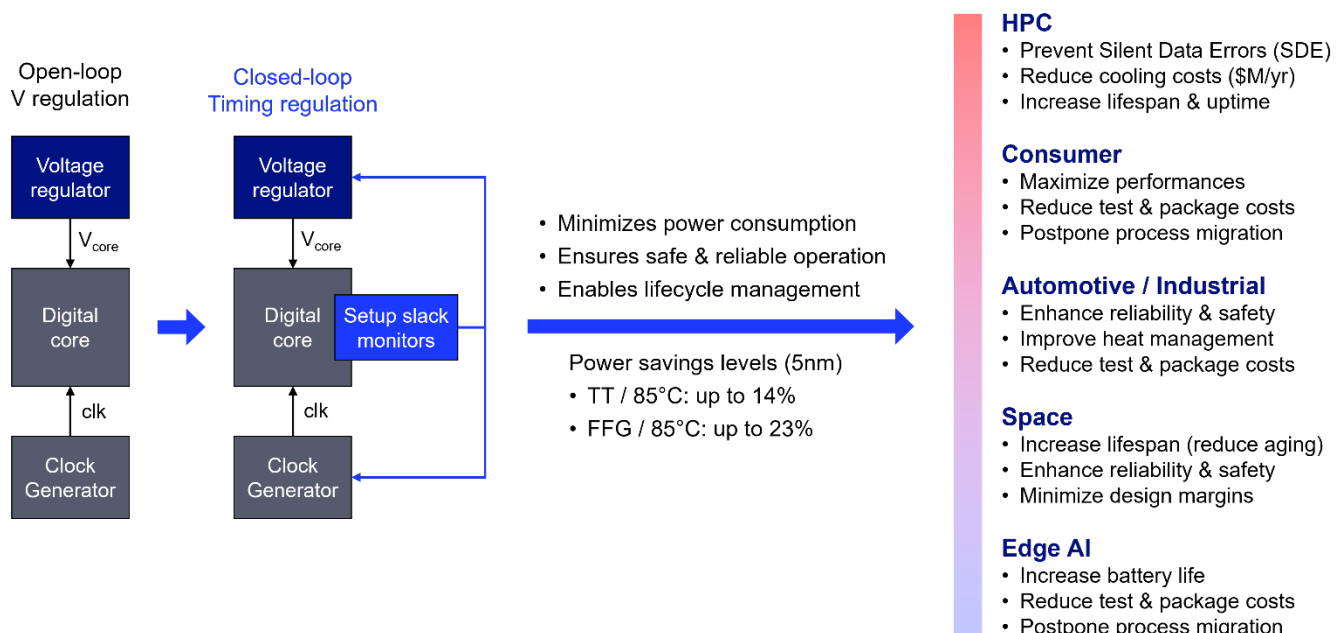


Figure 1 – Principle and benefits

Features

- Purely soft IP (synthesizable RTL)
- Fully based on standard cells
- Automated integration via TCL scripts
- Relies on patented setup slack monitors
- Fast & accurate sensing of setup slack margins
- Simultaneously monitoring of multiple setup slack margin levels
- Monitors any path as if it was a critical one
- Multiple path selection criteria: activity, IR-drop, data sensitivity...
- Worst paths are not monitored: neglectable impact on performances
- Monitors' setup at signoff phase: closer to silicon results
- Post tape-out, on-the-fly adjustable margins
- Compatible with reg-to-mem paths
- Silicon area overhead:
 - 0.1% of the gate count for cores ≤ 500 k FF
 - 0.035% of the gate count for cores > 3 M FF
- Voltage drop mitigation in less than 3 clock cycles
- Comes complete with control, interface and safety subblocks (see Figure 2)

Benefits

- A single solution for best-in-class AVFS, voltage drop mitigation and lifecycle management
- Monitor impacts of PVTA conditions at data level
- Power savings of timing regulation loop:
 - > 15% vs open-loop voltage regulation
 - > 10% vs PVT-based AVS loop
- Reliability enhancement thanks to reduced aging effects
- Safety improvement via ultra-fast protection mechanisms
- Minimize overdesign and specification spread
- Low dependency on process and EDA flow
- Calibration-less: no Look-Up Table (LUT)
- Silicon validation based on scan: no specific pin required; a digital tester is enough

Applications

- HPC SoCs
- Consumer CPUs
- Industrial & Automotive MCUs
- Edge-AI SoCs

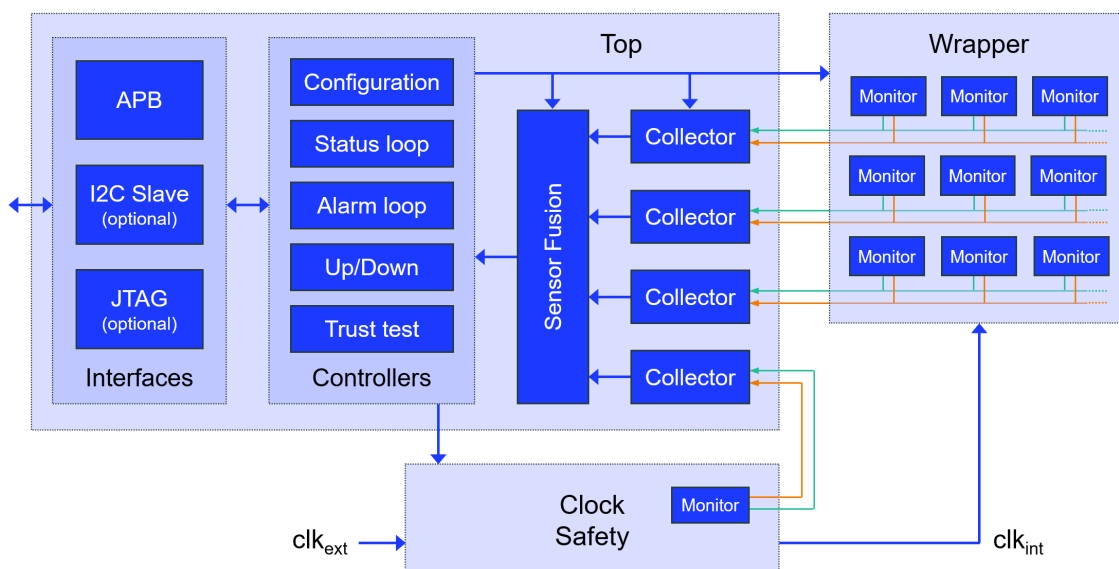


Figure 2 – Block-diagram

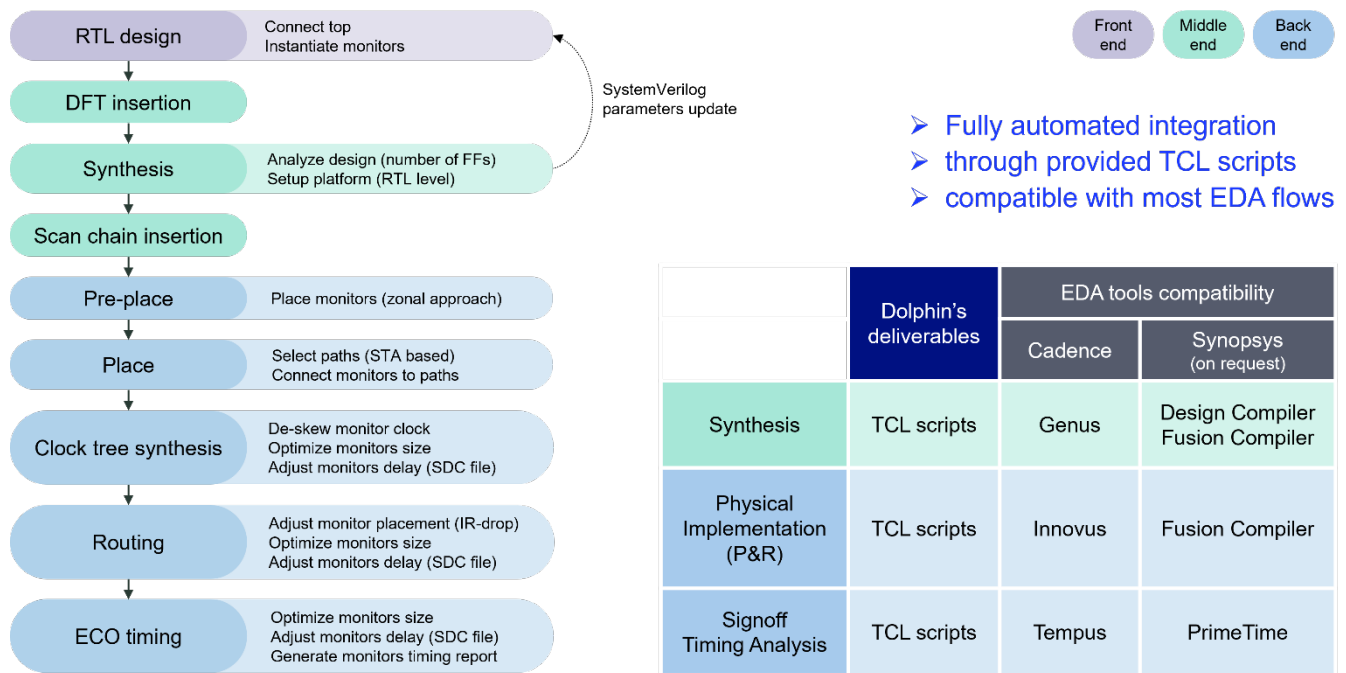


Figure 3 – Integration flow